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MAGGIE BAIRD (SENDER'S PRINTED NAME)

M. Baird (SIGNATURE)

PATENT APPLICATION
Docket No. 5087-080
CD03006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Nathan Moyal et al.

Serial No. 10/796,873 Examiner: Minh T. Nguyen

Confirmation No.: 2674

Filed: March 8, 2004 Group Art Unit: 2816

For: PHASE LOCKED LOOP OPERABLE OVER A WIDE FREQUENCY RANGE

TRANSMITTAL LETTER
OF APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Enclosed for filing in the above-referenced application are the following:

☒ Appellant's Brief (in Support of Notice of Appeal) in triplicate;
☒ **PTO Form 2038** authorizing credit card payment in the amount of **$500**;
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APPELLANT'S BRIEF

In accordance with CFR §41.37

Appeal is taken from the Examiner's Office Action mailed September 6, 2005 rejecting claims 1-20 in the above referenced application.

This Appeal Brief is in furtherance of the Notice of Appeal that was mailed on September 27, 2005.

The fees required under §41.37(a)(2) are dealt with in the accompanying paper entitled TRANSMITTAL OF APPEAL BRIEF and the document referenced therein.

This Brief is being filed in triplicate.

This Brief contains the items listed below under the headings listed below. These items appear in this Brief in the order listed below.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST --Reference 37 CFR §41.37(c)(1)(i)--

The real party in interest is Cypress Semiconductor Corp., to whom the subject application has been assigned.

II. RELATED APPEALS AND INTERFERENCES --Reference 37 CFR §41.37(c)(1)(ii)--

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, to the appellant's legal representative, or to the assignee.

III. STATUS OF CLAIMS --Reference 37 CFR §41.37(c)(1)(iii)--

The status of the claims in the subject application is as follows:

1. Claims presented: 1-20
2. Claims withdrawn from consideration but not cancelled: NONE
3. Claims canceled: none
4. Claims pending are: 1-20 of which:
   a. claims allowed: NONE
   b. claims rejected: 1-20

All the rejected claims, namely claims 1-20, are being appealed. The appealed claims are eligible for appeal, having been finally rejected.

IV. STATUS OF AMENDMENTS --Reference 37 CFR §41.37(c)(1)(iv)--

An amendment after final was filed on 09/27/05 in order to correct a minor grammatical irregularity in claim 1. By Office action dated 10/13/05 the examiner indicated that the amendment had been entered.

A second amendment after final was filed on 11/10/05 to change a very minor typographical error in claim 15. The change is non substantive in that it merely eliminates a word that was repeated. This amendment was discussed with the examiner on 11/15/05 by telephone and the examiner agreed that the change was non-substantive and that the amendment would be accepted; however, applicant has not (as of the time this brief was filed) received written confirmation that the amendment was accepted.

V. SUMMARY OF CLAIMED SUBJECT MATTER --Reference 37 CFR §41.37(c)(1)(v)--

The present invention relates to a Phase Locked Loop (PLL) that can operate over a wide frequency range and yet maintain a relatively constant loop gain. The PLL includes a Variable Frequency Oscillator (VFO), the gain profile of which can be varied. The frequency range over which the PLL operates is divided into a plurality of sub-ranges. When the frequency of the PLL moves between frequency ranges, the gain profile of the VFO is changed so that the loop gain remains within a pre-established range.

VI. GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL

--Reference 37 CFR §41.37(c)(1)(vi)--

A. Whether claims 1-3, 10-12, 15-16 and 18-20 are unpatentable under 35 U.S.C. § 102(b) in view of US Patent 5,686,864 issued to Martin et. al. All of the claims subject to this rejection are independent claims except claim 16.

B. Whether dependent claims 4-9, 13-14 and 17 are unpatentable under 35 U.S.C. § 103 in view of US Patent 5,686,864 issued to Martin et al.

VII. ARGUMENT --Reference 37 CFR §41.37(c)(1)(vii)--

All of the claims subject to the rejection under 35 U.S.C. § 102(b) (that is, claims 1-3, 10-12, 15-16 and 18-20) can be grouped together into a single group as they present the same issues relative to the cited reference.

Likewise all of the claims that were subject to the rejection under 35 U.S.C. § 103 (that is, claims 4-9, 13-14, and 17) can be grouped together and discussed as a single group as they present the same issues relative to the cited reference.

Argument relative the rejection under 35 U.S.C. § 102(b), that is, argument relative to the first group of claims:

These claims were all rejected under 35 U.S.C. § 102(b). Thus, the issue relative to these claims does not involve an issue of obviousness.

Some of the claims in the first group of claims are apparatus claims and others are method claims. However, with respect to the rejection based on the Martin reference, the same issues are raised by all the claims in the first group of claims. The language of claim 1 will be used in the following discussion as representative of the language in the apparatus claims and the language of claim 15 will be used as representative of the language in the method claims. It is noted that with respect to the issues being discussed, similar language can be found in each of the claims in the first group of claims.

Applicant is claiming a Phase Locked Loop (PLL) that includes a Variable Frequency Oscillator (VFO) that has a variable gain profile. Figure 2 shows a Voltage Controlled Oscillator (VCO) 203. It is noted that a VCO is a type of VFO (see specifications page 2 line 22). Figure 3 shows that the gain profile of the VCO 203 has three different gain curves designated "Gain Curve A", "Gain Curve B", and "Gain Curve C".

Applicant's circuit includes Gain Profile Control Logic 210 which switches the gain of the VCO 203 as the frequency of the PLL (shown in Figure 3) moves from sub-range A, to sub-range B, to sub-range C. The apparatus and method for changing the gain profile of the VFO as the frequency moves between sub-ranges is defined in the claims as follows:

Apparatus claim 1 recites:

> "a variable frequency oscillator (VFO) ...
> said PLL operating over a frequency range that includes a number of frequency sub-ranges ...
> said VFO having a variable gain profile, the gain profile of said VFO being controlled by gain control logic which sets the gain profile of said VFO so that the gain of the VFO remains within a desired range as the operation of said PLL moves between said frequency sub-ranges."

Method claim 15 recites:

> "changing the loop gain profile of said PLL when the operation of said PLL changes sub-ranges, said profile being changed to a profile that has a gain within pre-established limits over said frequency sub-range."

No such structure or method is shown in the Martin reference that was cited by the examiner. The cited Martin reference shows a first embodiment with a number of VCO circuits having different frequency ranges and a second embodiment showing a single VCO that has a variable frequency range.

When trying to lock onto a frequency, if the circuit cannot lock onto a frequency with one particular VCO (or with the VCO operating at a particular frequency), the circuit switches to a different VCO with a different frequency range (or it switches the frequency range of the VCO to a different frequency range).

The circuit shown in the Martin reference has a lock detect circuit 118. As indicated at column 2 lines 36 to 40, the lock detect circuit 118 determines whether the synthesizer 100 has locked onto a frequency with the currently enabled VCO circuit. If the synthesizer 100 has not locked onto a frequency:

> "VCO control circuit 114 continues to alternately enable and disable each of the plurality of VCO circuits 112 until the lock indicator signal 120 indicates that the synthesizer has locked on frequency with one of the VCO circuits". (*See* Martin, column 2, lines 43 *et. seq.*)

Nowhere, in the Martin reference, is there any discussion of the gain of the VCO circuits. **The term "gain" does not even appear in the Martin reference.** Martin is concerned only with selecting a VCO that can operate at an appropriate frequency (or with adjusting a VCO so that it can operate at a particular frequency range).

Figure 6 of Martin shows a VCO, the frequency range of which can be varied. However, the frequency range is varied based upon the output of the lock detect circuit 118 shown in Martin. The frequency range of the VCO is changed until the lock detection circuit 118 indicates that the circuit is in locked condition. In contrast to the way the circuit shown in Martin operates, in the applicant's circuit, the "gain control logic" sets the gain profile of said VFO so that the gain of the VFO remains within a desired range as the operation. The gain control logic is specifically recited in applicant's claim and no such logic is disclosed in the Martin reference.

Applicant's claims recite a combination of a single VFO that has a variable gain profile. Applicant's claims recite how an appropriate gain profile for the VFO is selected. A different gain profile for the VFO is selected as the circuit moves between frequency ranges. Changes in applicant's circuit are under control of "gain control logic". This is specifically recited in applicant's claims.

Applicant's claims recite that "the gain of the VFO remains within a desired range as the operation of the PLL mover between frequency ranges" (from claim 1). There is no suggestion whatsoever in Martin of maintaining gain within a particular range.

Since the cited Martin reference does not teach the combination claimed by the applicant, the rejection under 35 U.S.C. § 102(b) is not appropriate and it should be reversed.

Argument relative the rejection under 35 U.S.C. § 103, that is argument relative to the second group of claims (that is, dependent claims 4-9, 13-14 and 17):

All of the claims in the second group of claims are dependent claims. With respect to the Martin reference, each of the claims in this group of claims presents the same issue. Claim 4 which is dependent upon claim 1 is representative and will be used in the following discussion. It is noted that it is the language from the parent claim that the applicant is relying upon to distinguish these claims from the cited reference.

The arguments made above relative to the fact that Martin does not deal with selecting an appropriate gain profile are equally applicable to the rejection of the second group of claims under 35 U.S.C. 103 and the argument made above relative to the first group of claims are hereby incorporated by reference into this discussion of the rejection under 35 U.S.C. 103.

Since the Martin reference does not even mention the term "gain", it is clear that the teaching in the Martin reference does not relate to adjusting the gain profile of the VFO (or the VCO shown in Martin).

The examiner has cited only the Martin reference and this reference shows both a circuit with multiple VCOs and a circuit with a single VCO that can operate over multiple frequency ranges. The reference deals with selecting the frequency range of a VCO so that the circuit can operate in a locked condition.

As discussed above the Martin reference does not even mention the term "gain". The martin reference is not concerned with the gain of the VCO. The Martin reference is merely directed to selecting a VCO that can operate at a particular selected frequency or adjusting a VCO so that it can operate at a particular frequency. When the lock detection circuit 118 shown in Martin detects that the circuit is operating in an unlocked condition, different VCO circuits are tried until one is found that operates at the appropriate frequency (or as shown in Figure 6, the frequency range is changed until an appropriate frequency range is found). The circuit in Martin operates on a trial and error basis. Even in this respect, the teaching in Martin is contrary to the operation of the applicant's circuit in that in applicant's circuit, the gain of the VCR is changed when the operation moves between frequency sub-ranges.

Martin does not teach a circuit that includes "gain control logic" as recited in applicant's claims. There is no suggestion whatsoever in Martin of any "gain control" logic.

Applicant's claim 4, which is dependent on claim 1 recites (from claim 1) that:

> "the gain profile of said VFO being controlled by gain control logic which sets the gain profile of said VFO so that the gain of the VFO remains within a desired range as the operation of said PLL moves between said frequency sub-ranges."

There is no discussion in the Martin reference concerning "gain", hence, it can not be obvious from Martin to arrive at the applicant's combination.

Since the cited Martin reference does not suggest in anyway the combination claimed by the applicant, and since applicant's combination is not obvious in view of what is shown in the Martin reference, the rejection under 35 U.S.C. § 103 is not appropriate and it should be reversed.

VIII. CLAIMS APPENDIX --Reference 37 CFR §41.37(c)(1)(viii)--

The text of the claims on appeal is as follows:

1. A phase locked loop (PLL) system including

a phase frequency detector (PFD),

a filter, a variable frequency oscillator (VFO), and

a feedback loop including a frequency divider that has several divider values, said PLL operating over a frequency range that includes a number of frequency sub-ranges, the center frequency of each sub-range being determined by one of said divider values,

said VFO having a variable gain profile, the gain profile of said VFO being controlled by gain control logic which sets the gain profile of said VFO so that the gain of the VFO remains within a desired range as the operation of said PLL moves between said frequency sub-ranges.

2. A method of operating a phase locked loop (PLL) which operates over a frequency range that includes a number of frequency sub-ranges, said sub-ranges being established by the value of a frequency divider in a feedback loop,

said PLL including a variable frequency oscillator (VFO) the gain profile of which is variable in response to changing the value of selected components of said VFO,

said method including,

determining the particular setting of said selected components for each frequency sub-range that produces a selected gain profile that is within pre-established limits for each of said frequency sub-ranges, and

changing the settings of said selected components to the particular settings for each frequency sub-range when said PLL is set to operate within a particular sub-range.

3. A phase locked loop(PLL) system including

a phase frequency detector (PFD),

a filter, a variable frequency oscillator (VFO),

and a feedback loop including a frequency divider having a plurality of divide values,

said PLL operating over a frequency range that includes a plurality of frequency sub-ranges, each range being established by a divider value of said divider,

said VFO having variable gain profile, said variable gain profile having one value for each particular frequency sub-range which maintains the gain of said VFO within pre-established limits within said particular frequency sub-range, and

a logic circuit operable when the frequency of operation of said PLL changes frequency sub-range to change the gain profile of said VFO to a value which maintains said gain within pre-established limits over said frequency sub-range.

4. The system recited in claim 1 wherein said frequency range is from 2.4 GHz to 2.48 GHz.

5. The method in recited in claim 2 wherein said frequency range is from 2.4 GHz to 2.48 GHz.

6. The system of claim 1 wherein said desired range of gain is from 0.26GHz per volt to 0.325 GHz per volt.

7. The method of claim 2 wherein said pre-established limits are from 0.26GHz per volt to 0.325 GHz per volt.

8. The system in claim 1 wherein said frequency range is divided into three sub-ranges.

9. The method of claim 2 wherein said frequency range is divided into three sub-ranges.

10. A phase locked loop(PLL) including

a phase frequency detector (PFD),

a filter, a voltage controlled oscillator (VCO), and

a feedback loop including a frequency divider, said frequency divider having a plurality of divider values,

said PLL operating over a frequency range that includes a number of frequency sub-ranges, said VCO having a variable gain profile, and

means for changing the gain profile of said VCO when said, PLL changes operation between said frequency sub-ranges,

whereby the gain of said VCO is within pre-established limits over each frequency sub-range.

11. A method of operating a phase locked loop (PLL) which operates over a frequency range that includes a number of frequency sub-ranges, said PLL including a voltage controlled oscillator (VCO) the gain profile of which is variable, said method including:

a feedback loop having a frequency divider, said divider having a plurality of divider values that establish different frequency sub-ranges,

changing the frequency of operation of said PLL,

determining if said PLL is operating in a different frequency sub-range when the frequency of operation changes, and

when the frequency of operation of said PLL changes frequency sub-ranges, changing the gain profile of said VCO to a profile that is within pre-established limits over said frequency sub-range.

12. A phase locked loop (PLL) system which operates over a frequency range that includes a number of frequency sub-ranges established by the division provided by a frequency divider in a feedback loop, said PLL including

a variable frequency oscillator (VFO) the gain profile of which is variable,

a first circuit for changing the frequency of operation of said PLL,

a second circuit for determining if changes to the frequency of operation of said PLL has changed the frequency sub-range in which said PLL is operating, and

a third circuit operable when the frequency of operation of said PLL changes frequency sub-ranges to change the gain profile of said VFO to a profile that has a gain within pre-established limits over said frequency sub-range.

13. The system recited in claim 12 wherein said frequency range is from 2.4 Ghz to 2.48 Ghz.

14. The system of claim 1 wherein said pre-established limits of gain is from 0.26GHz per volt to 0.325 GHz per volt.

15. A method of operating a phase locked loop (PLL) which operates over a frequency range that includes a number of frequency sub-ranges, said frequency ranges being established by the value of a frequency divider in a feedback loop, said PLL including a variable frequency oscillator (VFO), said PLL having a loop gain profile which is variable, said method including,

determining if changes to the frequency of operation of said PLL has changed the frequency sub-range in which said PLL is operating, and

changing change the loop gain profile of said PLL when the operation of said PLL changes sub-ranges, said profile being changed to a profile that has a gain within pre-established limits over said frequency sub-range.

16. A phase locked loop (PLL) system recited in claim 12 wherein said third means includes gain control logic which changes the gain of said VFO when said PLL changes sub-ranges.

17. A phase locked loop (PLL) system recited in claim 12 wherein the overall gain of said system is substantially symmetrical around the center of said frequency range.

18. A phase locked loop(PLL) system including

a phase frequency detector (PFD),

a filter,

a variable frequency oscillator (VFO), and

a feedback loop including a frequency divider, which has a plurality of divider values, thereby establishing a plurality of frequency sub-ranges,

said PLL operating over a frequency range that includes a number of said frequency sub-ranges,

said PLL having a variable loop gain profile,

the loop gain profile of said PLL being controlled by gain profile control logic which sets the loop gain profile of said PLL so that the loop gain of the said PLL remains within a desired range as the operation of said PLL moves between said frequency sub-ranges.

19. The phase locked loop system recited in claim 18 wherein said loop gain profile is changed by changing the gain profile of said VFO.

20. The phase locked loop system recited in claim 18 wherein said VFO is a Voltage controlled oscillator (VCO).

IX. CONCLUSION

The Appellant respectfully requests that the examiner's rejections of the claims in group 1 and group 2 be reversed.

Respectfully submitted,

DATED: November 16, 2005

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